TRANSISTOR RANGE MARKER AND SWEEP GENERATOR FOR RADAR DISPLAY

By Samuel A. Schwartz

I. INTRODUCTION

The accuracy with which radar information on the cathode-ray-tube screen can be interpreted depends upon the precision of the associated range marker and sweep generator. Not only does the electronic circuitry described in this paper adequately perform the required generator function, but also several features inherent in the circuitry enhance overall radar operability. Notable among these features are the following:

1. Factory and field set-up adjustments are eliminated.
2. Range is easily converted from statute to nautical miles.
3. A low cost plug-in element (quartz crystal) provides overall accuracy.
4. The small, highly reliable circuits are easily maintained.

The generator provides both 1- and 5-mile markers which can be used either separately or together and are distinguished on the screen by different amplitudes. A range gate is also provided which has a period equivalent to either a 5- or a 25-mile range. The output amplitudes and polarities are compatible with the portable radar display equipment for which the generator was designed, and, if needed, other polarities and amplitudes can be obtained.

II. DESCRIPTION OF RANGE MARKER AND RANGE GATE CIRCUITRY

The generator, as shown in the block diagram of Fig. 1, consists of a precision timing oscillator and a cascade of binary divider circuits in combination with appropriate switching and output stages. Transistor type 2N2369, a high speed planar epitaxial switch, is used for all stages.

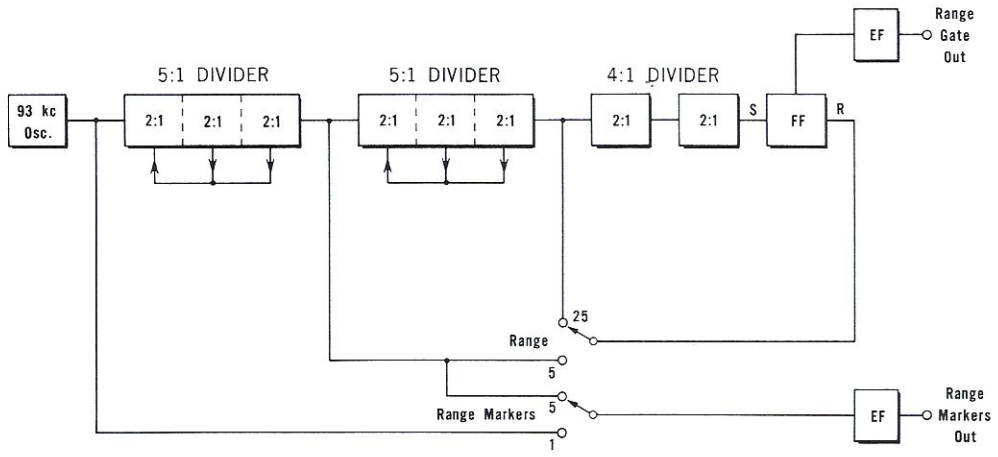

FIG. 1. Block Diagram of Range Marker and Range Gate Generator.

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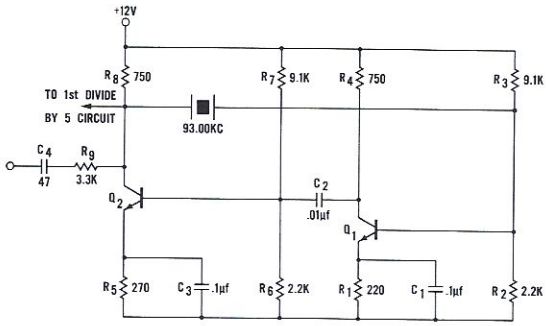
The timing oscillator determines overall range accuracy. Its operating frequency of 93 kc produces one cycle per radar mile so that ranging is marked in statute miles (based on the velocity of radio waves of 186,000 miles per second and the radar mile, consisting of a two-way path--transmission and return distance).

The oscillator, as shown schematically in Fig. 2, consists of a pair of Class-A, resistance-coupled amplifiers in cascade. The feedback path from the collector of the second stage to the base of the first stage contains a quartz, frequency-determining crystal operating in the series mode. Thus positive feedback is provided at the frequency of the crystal, and oscillations are maintained in the circuit. The oscillator comprises transistors Q_1 and Q_2 (type 2N2369) and their associated bias and collector load resistors. In order to provide maximum stage gain, the emitters are maintained at a-c ground by means of bypass capacitors. The voltage output at the collector of Q_2 has a sufficiently fast fall time to drive a binary divider without additional speed-up circuitry.



Q_1, Q_2=2N2369

FIG. 2. Schematic Diagram of Oscillator.

The divider chain is composed of eight cascaded binary stages which are interconnected with appropriate feedback paths to form two sets of 5:1 dividers and one 4:1 divider. The binary stages are identical except for the feedback connections and are composed of basic flip-flop circuits with the addition of diode steering to effect the 2:1 frequency division. An additional flip-flop following the divider chain operates as a set-reset bistable circuit and generates the range gate signal.

The two cascaded 5:1 dividers are identical in both circuit and operation. The first divider, however, operates at five times the rate of the second. The 5:1 dividers are composed of three cascaded binary stages with feedback from the second and third binaries into the first binary. In this manner the basic binary count of eight is permuted to a count of five. The first binary receives three pulses from the feedback paths. Therefore only five external pulses are required to complete one output cycle. The states of the individual flip-flops are shown in Fig. 3 in relation to the trigger pulses within each divide cycle. Upon completion of a division of five input pulses, the final states of the flip-flops are the same as the initial states preceding the count. Thus the divider is ready to accept the next group of input trigger pulses. The accompanying waveforms are obtained by comparing the state of a particular flip-flop with the trigger pulses in a sequential manner.

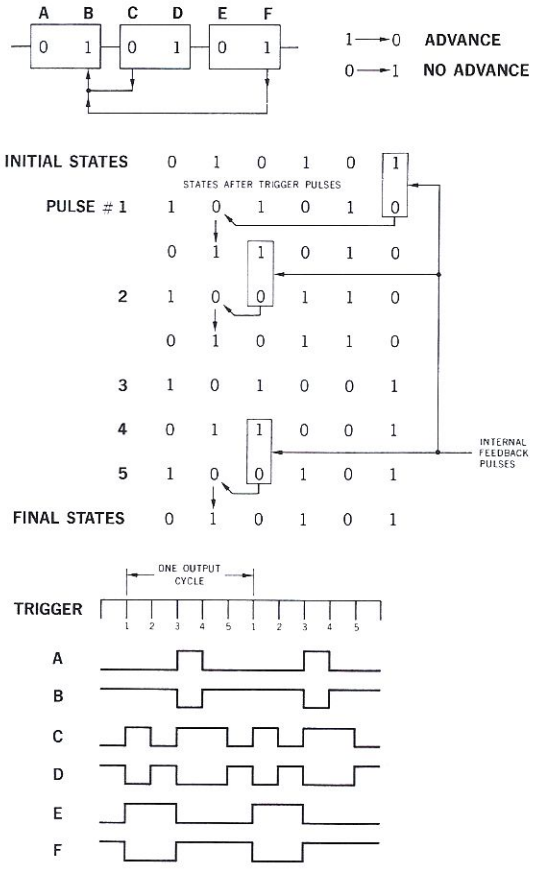

A B C D E F
1→0 ADVANCE
0→1 NO ADVANCE
INITIAL STATES 0 1 0 1 0 1
STATES AFTER TRIGGER PULSES
PULSE # 1 1 0 1 0 1 0
0 1 1 0 1 0
2 1 0 0 1 1 0
0 1 0 1 1 0
3 1 0 1 0 0 1
4 0 1 1 0 0 1
5 1 0 0 1 0 1
INTERNAL FEEDBACK PULSES
FINAL STATES 0 1 0 1 0 1
ONE OUTPUT CYCLE
TRIGGER
1 2 3 4 5 1 2 3 4 5
A
B
C
D
E
F

FIG. 3. Flip-Flop States and Waveforms in 5:1 Divider.

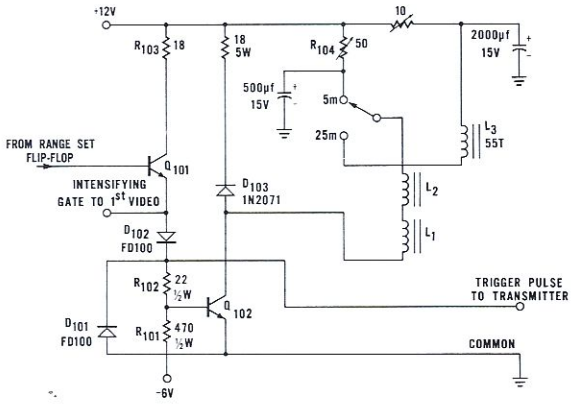
The 4:1 divider consists of two binary stages in cascade. Each binary is similar to those in the 5:1 dividers with the exception that no interconnecting feedback paths are required. The output of the 4:1 divider provides a "set" pulse for the gate-forming flip-flop. The "reset" pulse is obtained from the output of either the first or the second 5:1 divider, depending upon the range desired. If "reset" is obtained from the first 5:1 divider, the range gate will have a time duration equivalent to five radar miles, whereas an output from the second 5:1 divider results in a 25-mile gate.

Range markers are obtained by differentiating the square waves at the outputs of both the 93-kc oscillator and the first 5:1 divider. The outputs from the 93-kc oscillator and the 5:1 divider provide 1- and 5-mile markers, respectively. The markers are attenuated so that the 5-mile markers have a larger amplitude than the 1-mile markers and thus appear brighter on the radar display. The attenuators consist of adjustable pulse limiters rather than variable voltage dividers, and therefore produce range marker amplitude control without affecting pulse rise time. The range marker amplitude controls consist of variable resistors R_{11} and R_{12} for the 1- and 5-mile markers, respectively. Negative-going range markers are selected by diodes D_3 and D_4 and are preferred to positive-going markers since the rise time is faster in the negative direction.

The range markers are inverted in polarity in the amplifier stage comprising transistor Q_3 (2N2369) and then supplied by the collector output of Q_3 to the video amplifier for mixing with the intensifying gate and video signal. (See Fairchild APP-76, "A Transistor Video Amplifier for Radar Display.") The range gate signal at the emitter of Q_{101} clamps the collector of Q_3 to ground potential through D_{104}, preventing brightening of the blanked retrace.

III. DESCRIPTION OF SWEEP CIRCUITRY

The sweep generator (see Fig. 4 for schematic) contains a power transistor switch 2N2893 which connects the deflection yoke to a constant voltage source for a period determined by the selected range gate. As a result, the current tends to increase linearly in the deflection yoke, but because of the resistance of the yoke and switch, linearity is not perfect, and the sweep current sawtooth has a small exponential component. Compensation for nonlinearity is provided by a small saturable reactor in series with the deflection yoke, which causes the total circuit inductance to decrease as the deflection current increases. If resistance were not present in the yoke circuit, the deflection current would increase faster than required for perfect linearity, while the presence of circuit resistance causes the deflection current to increase too slowly for perfect linearity. Thus in the actual circuit, where resistance is present, the saturable reactor can be adjusted to compensate for the slowing effect of the resistance and provide a current wave of almost perfect linearity.



Q_{101}=2N2297
Q_{102}=2N2893

FIG. 4. Schematic Diagram of Sweep Generator.

Sawtooth currents of different slopes are produced on the 5- and 25-mile sweep ranges by varying the total circuit inductance; thus a constant supply voltage can be used. The circuit inductance necessary for operation on the 5-mile range consists of the deflection yoke inductance plus the saturable coil inductance.

For operation on the 25-mile range a second inductor is placed in series with the deflection yoke

and the saturable core inductor. This second inductor causes sufficient nonlinearity to compensate for the effect of its own resistance.

The sweep amplitude on both ranges is controlled by the d-c voltage supplied to the sweep circuit. On each range an adjustable resistor is placed between the d-c bus and the sweep circuit, and a bypass capacitor is connected across the sweep circuit. The average current required by each range results in a d-c drop across the resistor, which substracts from the d-c bus voltage and thus provides proper circuit d-c voltage. The bypass capacitor maintains the voltage constant and prevents the linearity-degrading effect which would otherwise be produced by adding resistance in the sweep current path. The range switch selects the appropriate resistor on each range.

The energy stored in the total circuit inductance at the end of the sweep period is dissipated between sweeps by a damping resistor. The resulting exponential decay of current through the deflection yoke produces a retrace deflection to the center of the cathode-ray-tube screen, which, however, does not appear since the electron beam is blanked out during the retrace interval. A diode in series with the damping resistor prevents current from flowing in the resistor during the sweep interval and thus reduces the current passing through the transistor switch.

The Fairchild planar 2N2893 transistor is an almost ideal switch for the deflection circuit for the following reasons:

1. It has a very low I_{CEX} even at high temperatures.* A higher I_{CEX} would cause variations in the starting position of each sweep which would appear as a small circle or "hole" around the screen center in the PPI display. Another result of higher I_{CEX} would be minor distortion of target shape, increasing for targets approaching zero range.

2. The β of the 2N2893 is adequate even at the 2-amp. peak current level so that saturation can be maintained without excessive overdrive. Thus the switch driver function can be handled adequately by the Fairchild planar 2N2297.

3. The 2N2893 LV_{CEO} rating of 80 volts is more than adequate to prevent failure due to breakdown at the peak voltage of 50 volts, which appears across the transistor at the start of the retrace interval.

4. The small forward saturation voltage drop across the 2N2893 causes very small device dissipation. Furthermore, the saturable reactor previously described easily compensates for this voltage drop, since it is equivalent to a switch "on" resistance.

5. The fast turn-off (in the range of submicroseconds) of the 2N2893, although not required for proper circuit performance, is advantageous from the device standpoint because it reduces dissipation during the turn-off interval when relatively high currents and voltages are available simultaneously.

The output switch transistor, Q_{102}, is maintained in the "on" condition by base current drive provided by the emitter current of the driver transistor, Q_{101}. Resistor R_{102} limits the base drive current. A positive-going sweep gate from the gate-forming flip-flop drives the base of Q_{101} during the sweep interval. During the retrace interval, the base voltage of Q_{101} goes essentially to zero (ground) while the emitter may go to -0.7 volt. Diode D_{101} allows the cathode end of diode D_{102} to go simultaneously to -0.7 volt. The voltage drop across D_{102} is zero since no current flows through it or from the emitter of Q_{101}. The resulting absence of dissipation in the driver transistor during the retrace interval offsets the rather high driver dissipation during the sweep interval so that the overall dissipation is safe. Resistor R_{103} in

* Typical value: 7 μA at 150°C, V_{CE} = 60 V, V_{BE} = -2 V.

the collector circuit further reduces the 2N2297 driver transistor dissipation. The resistance of R_{103} is low enough to prevent saturation of Q_{101} so that the full transistor β is available and hence loading on the gate-forming flip-flop by the driver stage is small.

During the retrace interval a reverse bias on the base of the switch transistor Q_{102} is established by the network of D_{101}, R_{101} and R_{102} across the -6 volt bias supply.

IV. DESIGN CONSIDERATION FOR THE RANGE MARKER AND SWEEP GENERATOR

The range marker and sweep generator circuits are designed to operate from the supply voltages of +12 and -6 volts common to other circuits in the radar. Power supply regulators maintain these voltages within $\pm$ 2% despite wide variation of input line voltage. This degree of supply regulation is not required by the crystal oscillator, flip-flops, and range marker inverter, but it is required by the sweep circuit for maintaining constant sweep amplitude.

Detailed designs of the crystal oscillator, flip-flops, and range marker inverter are described in numerous texts on transistor circuit design and are therefore not covered here, but the less commonplace deflection circuit design is covered.

The design of the sweep output stage is based on the known or extrapolated deflection yoke peak energy requirement for a cathode-ray tube operating under a given set of conditions. As an example, for a tube with a 52° deflection angle operating at 6 KV on the second anode, the peak energy stored per cycle in the magnetic field of the deflection yoke would be 0.56 millijoules. The required value of yoke inductance for this value of peak energy may be found from the following equation.

$$L_y = \frac{V^2 t_s^2}{2W_m}$$

(See Appendix Eq. (9A))

The value of inductance should be selected for the minimum range so that range time, t_s, will be minimum. For the 5-mile range, t_s = 53.8 μsec. For longer ranges extra inductance is added in series with the yoke inductance to reduce the rate of rise of the deflection current. The voltage, V, applied across the yoke by the switch transistor should be somewhat less than the available supply voltage to allow for the voltage drop across the sweep amplitude control and the linearity-correction inductance. With a supply voltage of 12 volts, a reasonable value for the yoke voltage is 10 volts. The yoke inductance may thus be calculated for the conditions given above.

$$L_y = \frac{10^2 (53.8 \times 10^{-6})^2}{2(0.56 \times 10^{-3})}$$

$$= 258\ \mu h$$

The peak deflection current, which is also the peak switch transistor current, is

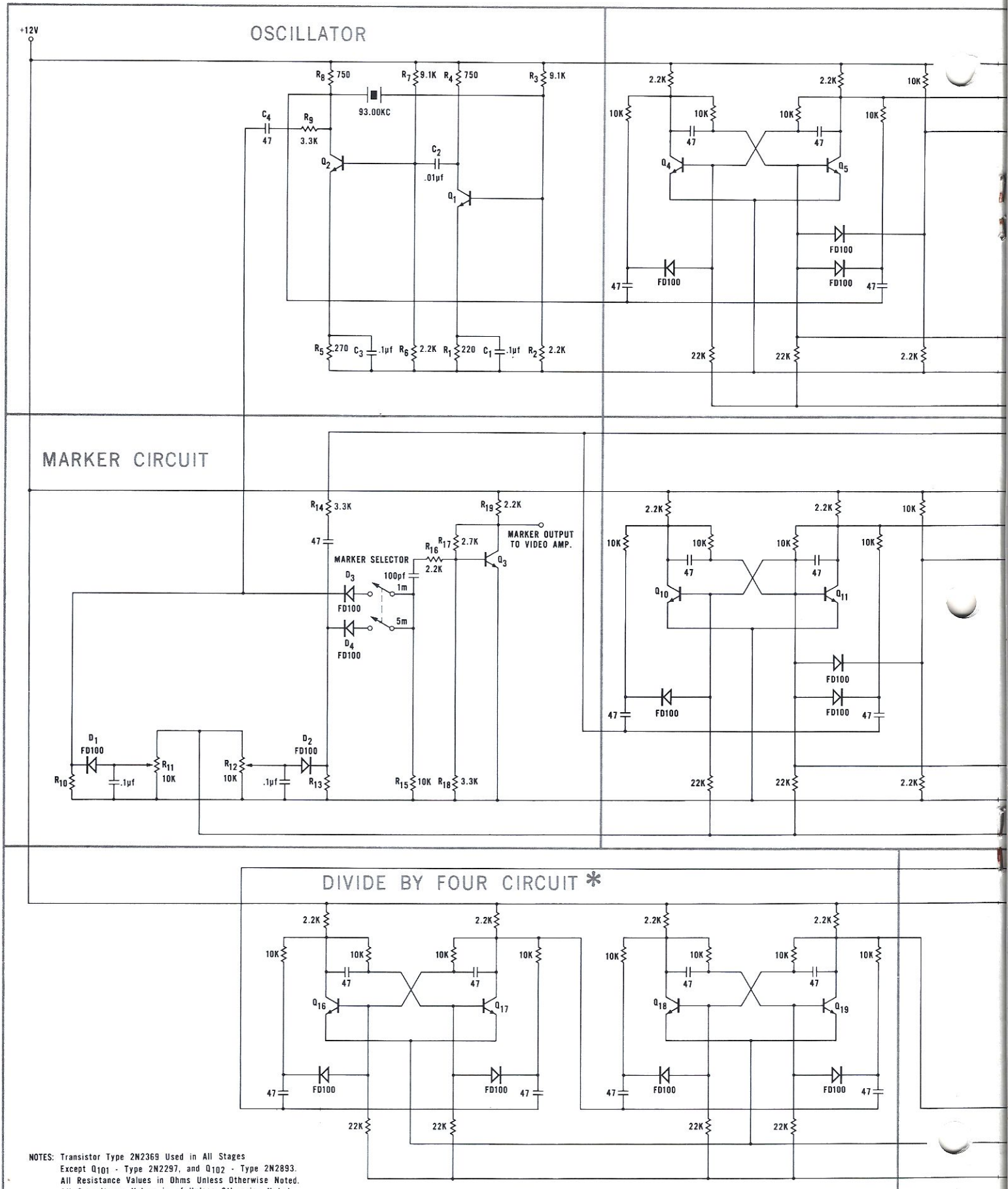
$$i_p = \sqrt{\frac{2W_m}{L_y}}$$

(See Appendix Eq. (8A))

$$= \sqrt{\frac{2(0.56 \times 10^{-3})}{258 \times 10^{-6}}}$$

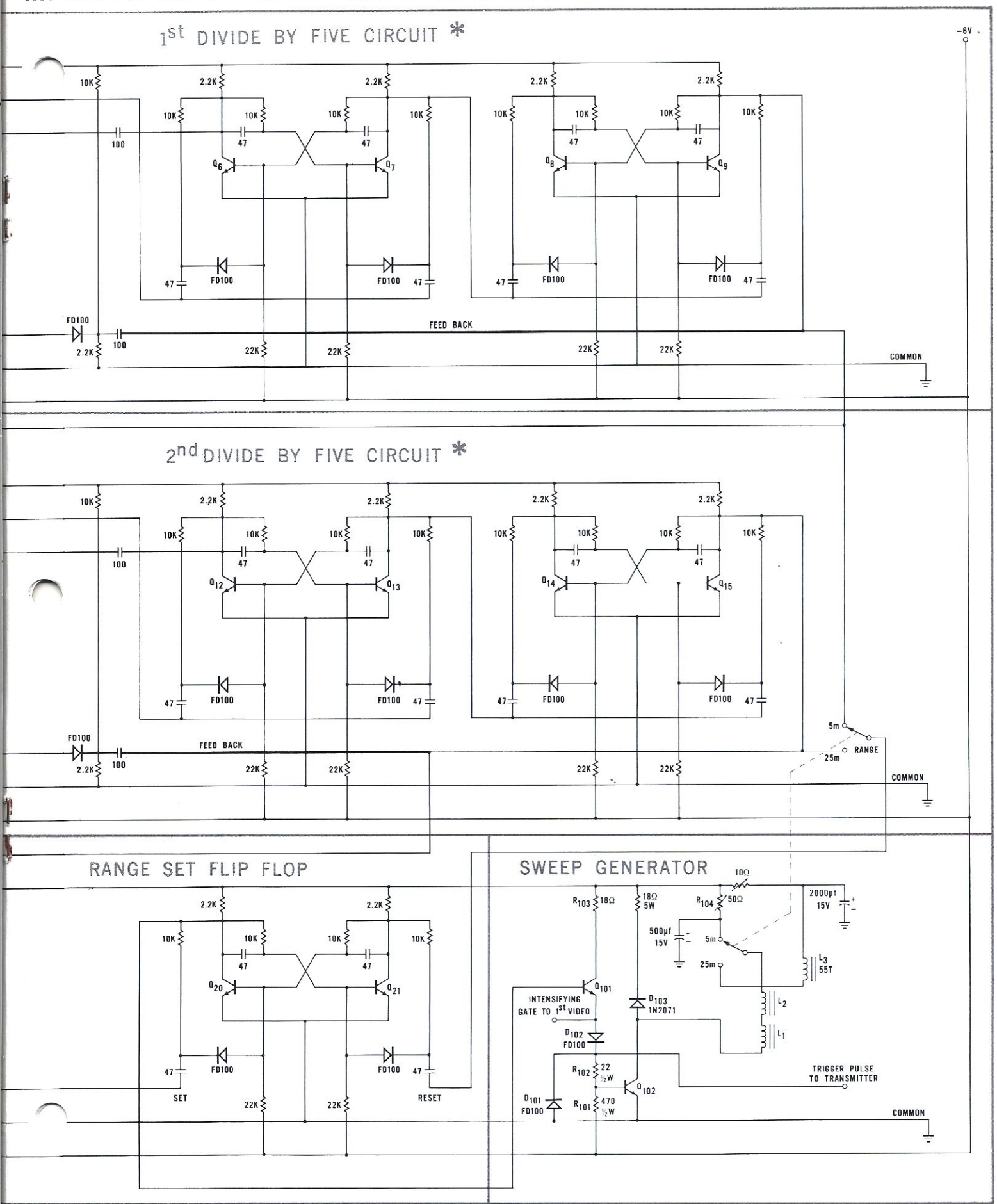
$$= 2.08\ A$$

SCHEMATIC DIAGRAM OF RANGE



NOTES: Transistor Type 2N2369 Used in All Stages
Except Q_{101} - Type 2N2297, and Q_{102} - Type 2N2893.
All Resistance Values in Ohms Unless Otherwise Noted.
All Capacitance Values in pf Unless Otherwise Noted.
* May be Integrated with Micrologic, See Page 11.

MARKER AND SWEEP GATE GENERATOR



The sweep amplitude control adjusts d-c voltage applied to the sweep circuit and thus controls the yoke voltage, V. The large bypass capacitor across the deflection yoke and transistor switch provides integration of the sweep current and thus allows a steady d-c current to flow through the sweep amplitude control resistance. The average, or d-c, current required by the circuit on the 5-mile range is

$$\begin{aligned} i_{d\text{-}c} &= \left(i_p/2\right) \text{x (sweep duty cycle)} \\ &= \left(i_p/2\right) \text{(sweep time) (prf)} \\ &= \left(2.08/2\right)(53.8 \times 10^{-6})\ (930) \\ &= 52 \text{ mA} \end{aligned}$$

The above value of d-c current is based on a circuit supply voltage of 10 volts. Therefore an amplitude control potentiometer of 50 ohms will allow adjustment of the voltage from approximately 9.4 volts up to the full supply voltage of 12 volts.

If the percentage change in bypass capacitor voltage, Δe_c, due to the flow of sweep current is held at or below 1% of the total bypass capacitor voltage, the size of the capacitor may be obtained as follows:

$$\Delta e_c = .01\, e_c$$

$$\Delta e_c = \frac{1}{C}\int_0^{t_s} (\Delta i_c)\,dt$$

$$\Delta i_c = \frac{Vt}{L}$$

$$C = \frac{1}{\Delta e_c}\int_0^{t_s} \frac{Vt}{L}\,dt$$

$$C = V(t_s)^2 \Big/ 2L\Delta e_c$$

$$= \frac{10\left(53.8 \times 10^{-6}\right)^2}{2(258 \times 10^{-6})\ (.01)\ (10)}$$

$$= 562\ \mu f$$

The total circuit inductance required for the 25-mile range is five times that needed for the 5-mile range. Thus the peak deflection current attains a value of 2.08 A in 269 μsec. An inductance of 1.032 mh, or four times the yoke inductance, is added in series with the yoke inductance to produce the desired value of total circuit inductance. The average current required by the circuit will increase by a factor of five over that required on the 5-mile range. Thus the value of the amplitude control resistance will be reduced by a factor of five down to 10 ohms, while the circuit bypass capacitor must be increased by a factor of five to approximately 3,000 μf.

The construction of the series inductor for the 25-mile range is such that it is nonlinear with current. By this expedient, the change in its inductance is made to compensate for its resistive component and thus not degrade the linear current sawtooth through it. The drawings in Fig. 5 show a typical construction for the linearity compensation coils as required in the sweep circuitry.

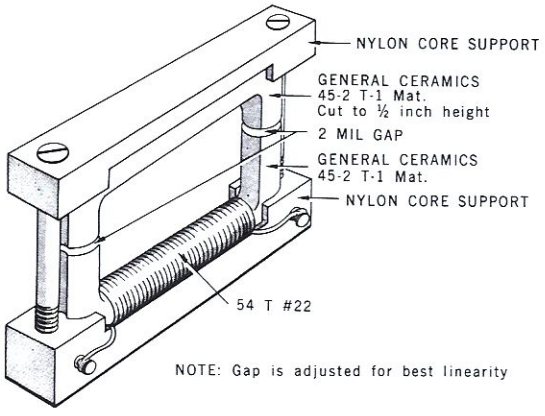


FIG. 5a. Long Range Linearity Compensation Coil.

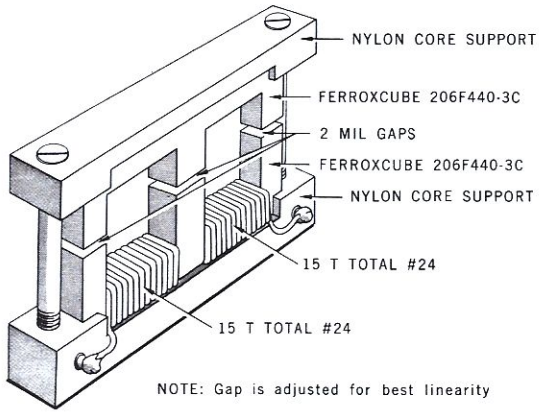


FIG. 5b. Short Range Linearity Compensation Coil.

The yoke-damping resistance must be large enough to cause the yoke current to decay to an insignificantly small value during the retrace interval and small enough to limit the peak transistor voltage, to V_{CE} max. at the start of retrace. In order to limit the transistor voltage, V_{CE}, to 50 volts, the peak yoke voltage must be (50 - 12) or 38 volts. Since the peak deflection current flows through the yoke-damping resistance at the start of retrace, the required value of resistance is 38/2.08, or 18.3 ohms. The resistor must have a power rating high enough for the longest sweep range since all of the yoke energy is dissipated in the resistor.

$$P = W_m \times prf$$

$$= (1/2)\, L(i_p)^2 \times prf$$

$$= (1/2)(258 + 1032) \times 10^{-6} (2.08)^2 (930)$$

$$= 2.59 \text{ watts}$$

Using a damping resistance of 18.3 ohms it is necessary to determine the decayed value of current at the end of the shortest retrace time occurring with the longest range.

$$i_r = i_p \epsilon^{-R_D tr / L_y}$$

(See Appendix Eq. (13A))

$$t = \frac{1}{prf} - t_s \quad \text{(25 mile range)}$$

$$t = \frac{1}{930} - 269 \times 10^{-6} = (1075 - 269) \times 10^{-6}$$

$$= 806\ \mu\text{sec}$$

$$i_r = 2.08\, \epsilon^{-18.3 \times 806 \times 10^{-6} / 1290 \times 10^{-6}}$$

$$= 2.08\, \epsilon^{-11.5} = 21.2\ \mu\text{A}$$

At the start of the sweep this value of retrace current offsets only 0.001% of the full sweep, which is inconsequential. The 18.3-ohm resistance is therefore sufficient.

The output transistor switch is assumed to have a minimum forced β of 20 while it is maintained in saturation by the driver stage. Thus the driver design follows a conventional emitter-follower stage with a current output capability of approximately 0.1 A.

V. APPENDIX

1. Analysis of deflection yoke drive

The sweep generator, operating in the switching mode, is analyzed below where the equivalent circuit consists of a voltage source, a switch, and the inductive and resistive components of the deflection yoke (Fig. 1A).

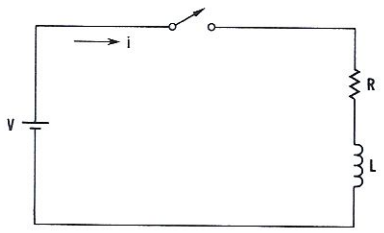


FIG. 1A. Equivalent Circuit of Yoke and Sweep Generator.

$$iR + L\frac{di}{dt} = V$$

$$RI(s) + L\left[sI(s) - I(0)\right] = V/s$$

$$RI(s) + LsI(s) - LI(0) = V/s$$

$$I(s)\left[R + sL\right] = (V/s) + LI(0) \qquad (1A)$$

It is essential that the initial current I(0) at the start of sweep be zero so that the trace will start at the center of the screen.

$$\therefore I(s) = \frac{V}{s} \cdot \frac{1}{R + sL}$$

$$= \frac{V}{L} \cdot \frac{1}{s(s + R/L)}$$

$$i(t) = \frac{V}{L}\frac{1}{R/L}\left(1 - \epsilon^{-Rt/L}\right)$$

$$= \frac{V}{L}\frac{L}{R}\left(1 - \epsilon^{-Rt/L}\right)$$

$$i(t) = \frac{V}{R}\left(1 - \epsilon^{-Rt/L}\right) \qquad (2A)$$

From Eq. (2A) it may be seen that the desired linear rise of current is degraded by circuit resistance, and an exponentially increasing current is produced. If an element equal to -R is added to the circuit, Eq. (1A) becomes

$$iR + i(-R) + L\frac{di}{dt} = V$$

$$L\frac{di}{dt} = V$$

$$L\left[sI(s) - I(0)\right] = V/s$$

$$LsI(s) - LI(0) = V/s$$

$$LsI(s) = (V/s) + LI(0) \qquad (3A)$$

The initial current I(0) is zero as stated previously.

$$LsI(s) = V/s$$

$$I(s) = (V/L)(1/s^2)$$

$$i(t) = Vt/L \qquad (4A)$$

The peak value of the linear current sawtooth, i_p, is defined at the end of the trace period, t_s, so that

$$i_p = \frac{V}{L}(t_s) \qquad (5A)$$

The value of deflection yoke inductance is

$$L_y = \frac{V}{i_p}(t_s) \qquad (6A)$$

The deflection requirement for a cathode-ray tube may be defined in terms of the energy stored in the magnetic field of the deflection yoke at the end of the trace period when maximum deflection current is present.

$$W_m = (1/2)\, L_y (i_p)^2 \qquad (7A)$$

$$i_p = \sqrt{2W_m/L_y} \qquad (8A)$$

Substitution of Eq. (8A) in Eq. (6A) results in the equation for the deflection yoke inductance, L_y, as a function of the stored energy, W_m.

$$L_y = \frac{Vt_s}{\sqrt{2W_m/L_y}} = \frac{V^2(t_s)^2}{2W_m} \qquad (9A)$$

Upon completion of the sweep interval at the time t_s the maximum deflection current, i_p, must decay to zero or to an insignificantly small value before the next consecutive sweep can occur. The energy stored in the yoke is dissipated during the retrace interval in a damping resistance. The equivalent circuit during retrace, assuming the drop across the damper diode is constant, is shown below in Fig. 2A.

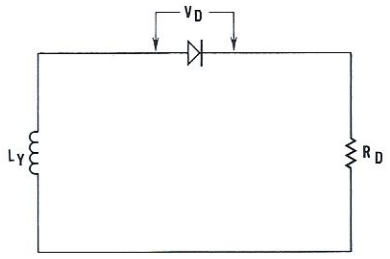


FIG. 2A. Equivalent Circuit During Retrace.

$$L_y\frac{di_p}{dt} + V_D + iR_D = 0$$

$$L_y\left[sI(s) - I(0)\right] + V_D + R_DI(s) = 0$$

$$sL_yI(s) - L_yI(0) + V_D + R_DI(s) = 0$$

$$I(s)\left[sL_y + R_D\right] = L_yI(0) - V_D$$

$$I(s) = \left[L_yI(0) - V_D\right]\Big/\left[sL_y + R_D\right]$$

$$= \left[I(0) - V_D/L_y\right]\Big/\left[s + R_D/L_y\right] \qquad (10A)$$

$$i(t) = \left[I(0) - V_D/L_y\right]\epsilon^{-R_Dt/L_y} \qquad (11A)$$

The current at the start of retrace is the same as that at the end of trace so that

$$i_p = I(0) - V_D/L_y \qquad (12A)$$

The retrace current is thus defined by

$$i(t) = i_p\,\epsilon^{-R_Dt/L_y} \qquad (13A)$$

2. Frequency divider using integrated circuits

The divider chain within the range marker and sweep generator may be implemented by the use of Fairchild Micrologic half-shift register elements, which are referred to as Part Nos. 905 and 906 with and without inverter, respectively. As with the binary divider described in this paper, the dividers are grouped into two 5:1 dividers and one 4:1 divider.

Each half-shift element consists of a double-gated flip-flop with an inverter. Counting or division is performed by the master-slave technique. The only components required in addition to the Micrologic elements are a capacitor and clamping diode at the input to the first divider. The resulting clamping circuit causes the input square wave to swing in the positive direction as required by the dividers.

The output voltage from the last divider stage in the 4:1 divider is 0.8 volts peak-to-peak, which is insufficient for driving the gate-forming flip-flop. Therefore, a transistor inverter should be added for raising the output level high enough to set the flip-flop. Similarly, an inverter at the output of both 5:1 dividers will provide suitable levels for resetting the flip-flop as well as high level range markers.

The wiring diagram for the divider is shown in Fig. 3A.

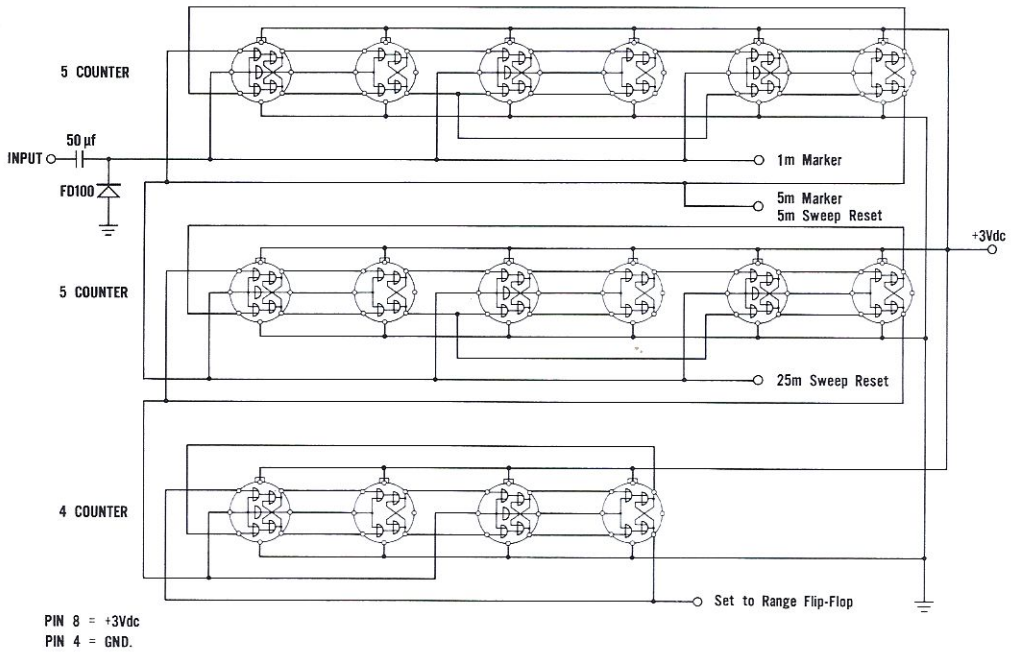


FIG. 3A. Frequency Divider Using Micrologic Elements.

CONCLUSION

The major circuitry in a radar indicator can be constructed from all-silicon planar transistors for high reliability. In addition, use of Micrologic elements for logic functions permits considerable reduction in size of circuitry. Other ranges can be incorporated into the radar for specific applications by the use of additional counting stages.

This application note is one of a series describing a small X-band radar set suitable for use in navigation and weather reconnaissance service which was constructed in the Fairchild Semiconductor Applications Laboratory. The individual sections of this equipment are described in APP-76 through APP-81. (These notes will be distributed as they become available.)

ACKNOWLEDGEMENT

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LIST OF SYMBOLS

C	Capacitance of bypass capacitor
Δe_c	Percentage change in bypass capacitor voltage due to flow of sweep current
Δi_c	Change in sweep current
e_c	Bypass capacitor voltage
i_{d-c}	D-C current through sweep amplitude control resistance
i_p	Peak deflection current; peak switch transistor current; peak value of linear current sawtooth
L_y	Yoke inductance
P	Power rating of damping resistor
R_D	Damping resistance
t_s	Range time
V	Yoke voltage
V_D	Voltage drop across damping diode
W_m	Peak energy stored in magnetic field of deflection yoke at end of trace period